WHAT IS CLAIMED IS:

1. A method for fabricating a stagger type thin film transistor substrate comprising the process of forming a resist pattern with different thicknesses in different areas by performing exposure once on a resist with a half tone mask.

2. The method for fabricating a stagger type thin film transistor substrate according to claim 1, wherein a resist pattern which masks a drain bus-line formed area on the thin film transistor substrate where a drain bus-line is to be formed and a thin film transistor formed area on the thin film transistor substrate where a thin film transistor is to be formed and in which the thickness of the resist in a channel formed area in the thin film transistor formed area where a channel for the thin film transistor is to be formed differs from the thickness of the resist in the drain bus-line formed area and the thin film transistor formed area other than the channel formed area is formed by performing exposure once on the resist with the half tone mask.

3. The method for fabricating a stagger type thin film transistor substrate according to claim 1, wherein a resist pattern which masks a gate bus-line formed area on the thin film transistor substrate where a gate bus-line is to be formed and a pixel electrode formed area on the thin film transistor substrate where a pixel electrode is to be formed and in which the thickness of the resist in the gate bus-line formed area

differs from the thickness of the resist in the pixel electrode formed area is formed by performing exposure once on the resist with the half tone mask.

4. A method for fabricating a stagger type thin film transistor substrate, the method comprising the processes of:

forming a resist on a drain bus-line layer formed over an operation layer over a substrate;

performing exposure on the resist with a half tone mask for forming a resist pattern in a drain bus-line formed area on the thin film transistor substrate where a drain bus-line is to be formed and a thin film transistor formed area on the thin film transistor substrate where a thin film transistor is to be formed, the resist pattern being thinner only in a channel formed area where a channel for the thin film transistor is to be formed;

etching the drain bus-line layer with the resist pattern;

ashing the resist pattern until removal of the thin resist formed in the channel formed area is completed; and

channel-etching the operation layer with the resist pattern which remains after the ashing.

5. The method for fabricating a stagger type thin film transistor substrate according to claim 4, wherein in the process of forming the resist on the drain bus-line layer formed over the operation layer over the substrate, a light shading film

is formed between the substrate and the operation layer and the resist is formed on the drain bus-line layer over the operation layer.

6. The method for fabricating a stagger type thin film transistor substrate according to claim 4, further comprising, after the process of channel-etching the operation layer with the resist pattern which remains after the ashing, the processes of:

removing the resist pattern which remains after the ashing, forming an insulating film on an entire surface, and making a contact hole which reaches the drain bus-line layer in the insulating film;

forming an irregular layer for scattering incident light on the entire surface except a gate bus-line formed area on the thin film transistor substrate where a gate bus-line is to be formed and an area where the contact hole is made;

forming a gate bus-line layer and forming a resist pattern which masks the gate bus-line formed area and a pixel electrode formed area on the thin film transistor substrate where a pixel electrode is to be formed on the gate bus-line layer; and

etching the gate bus-line layer with the resist pattern.

7. A method for fabricating a stagger type thin film transistor substrate, the method comprising the processes of:

forming a drain bus-line layer over an operation layer

formed over a substrate, forming a drain bus-line on the thin film transistor substrate by etching, and forming a channel area for a thin film transistor to be formed on the thin film transistor substrate in the operation layer by the etching;

forming an insulating film and making a contact hole which reaches the drain bus-line layer in the insulating film;

forming a transparent conductive film layer and a gate bus-line layer in that order on the insulating film in which the contact hole is made, and forming a resist pattern , in which a resist in a pixel electrode formed area on the thin film transistor substrate where a pixel electrode is to be formed is thinner than the resist in a gate bus-line formed area on the thin film transistor substrate where a gate bus-line is to be formed, in the gate bus-line formed area and the pixel electrode formed area on the gate bus-line layer by the use of a half tone mask;

etching the gate bus-line layer and the transparent conductive film layer with the resist pattern;

ashing the resist pattern until removal of the thin resist formed in the pixel electrode formed area is completed; and

etching the gate bus-line layer in the pixel electrode formed area with the resist pattern which remains after the ashing.

8. The method for fabricating a stagger type thin film transistor substrate according to claim 7, wherein in the process

of forming the drain bus-line layer over the operation layer formed over the substrate, forming the drain bus-line on the thin film transistor substrate, and forming the channel area for the thin film transistor to be formed on the thin film transistor substrate in the operation layer, a light shading film is formed between the substrate and the operation layer, the drain bus-line layer is formed over the operation layer, the drain bus-line is formed on the thin film transistor substrate, and the channel area for the thin film transistor to be formed on the thin film transistor substrate is formed in the operation layer.

9. The method for fabricating a stagger type thin film transistor substrate according to claim 7, wherein in the process of forming the insulating film and making the contact hole which reaches the drain bus-line layer in the insulating film, a contact hole for bringing the drain bus-line layer into contact with the transparent conductive film layer and a contact hole for a terminal on the thin film transistor substrate are made.

10. A method for fabricating a stagger type thin film transistor substrate, the method comprising the processes of:

forming a drain bus-line layer over an operation layer formed over a substrate, forming a drain bus-line on the thin film transistor substrate by etching, and forming a channel area for a thin film transistor to be formed on the thin film transistor substrate in the operation layer by the etching;

forming an insulating film and a transparent conductive film layer in that order;

forming a resist pattern in which an opening is made over a contact hole to be made in the insulating film and in which a resist is thicker only in a pixel electrode formed area on the thin film transistor substrate where a pixel electrode is to be formed on the transparent conductive film layer with a half tone mask;

etching the insulating film and the transparent conductive film layer with the resist pattern for making the contact hole;

ashing the resist pattern until removal of the thin resist formed in areas other than the pixel electrode formed area is completed; and

etching the transparent conductive film layer with the resist pattern which remains after the ashing.

11. A stagger type thin film transistor substrate in which each of a source and a drain of a thin film transistor has a laminated structure including a silicon semiconductor layer, a silicon semiconductor layer containing impurities, and a metal layer formed in that order and in which a gate insulator of the thin film transistor is formed on the source and the drain.

12. The stagger type thin film transistor substrate according to claim 11, wherein a pixel electrode is connected

to the source via a contact hole made in the gate insulator on the source.

13. The stagger type thin film transistor substrate according to claim 12, wherein a gate electrode of the thin film transistor formed on the gate insulator has a laminated structure including two layers of different electrode materials and the pixel electrode connected to the source is made of an electrode material used in a lower layer of the gate electrode.

14. The stagger type thin film transistor substrate according to claim 13, wherein the lower layer of the gate electrode is a transparent conductive film.